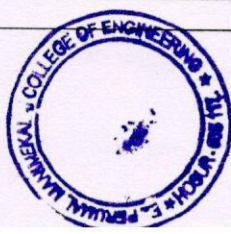




Program		B.E		Class		EEE	
Year		II		Semester		III	
Faculty Name		Dr.K.KALAISELVAN		DATE		17.06.2019	
Subject Code		EE8351		Subject Title		DIGITAL LOGIC CIRCUITS	
Week	Lecture Date	Day	Period	Topics	Teaching Method	Students Preparation	Reference Book
<b>UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES</b>							
1	17-Jun-19	MON	2,6	Review of number systems	Lecture	ASS-I	T1
	18-Jun-19	TUE	2	Binary codes	Lecture		T1
	19-Jun-19	WED	8	Error detection and correction codes	Tutorial		T1
	20-Jun-19	THU	4,6	Digital Logic Families: RTL	Lecture		T1
	21-Jun-19	FRI	1	DTL	Lecture		T1
	22-Jun-19	SAT	3	TTL	Lecture		T1
	25-Jun-19	TUE	2	ECL	Lecture		T1
2	26-Jun-19	WED	8	MOS Families-Operation	Lecture	T1	
	27-Jun-19	THU	4,6	Characteristics of digital logic family	Lecture	T1	
<b>UNIT II COMBINATIONAL CIRCUITS</b>							
2	28-Jun-19	FRI	8	Combinational logic	Lecture	ASS-I	T1
	29-Jun-19	SAT	3	Representation of logic functions, SOP	Lecture		T1
	1-Jul-19	MON	2	K-map representations	Lecture		T1
3	2-Jul-19	TUE	1	Minimization using K-maps	Lecture	ASS-I	T1
	3-Jul-19	WED	4	Simplification and implementation of	Lecture		T2
	4-Jul-19	THU	4,6	Multiplexers and Demultiplexers	Lecture		T1
4	5-Jul-19	FRI	8	Code converters	PPT	ASS-I	T1
	6-Jul-19	SAT	3				
	6-Jul-19	SAT	8	Adders and subtractors	Lecture		
	8-Jul-19	MON	2	Encoder and Decoder	Tutorial		
	9-Jul-19	TUE	1	Quine McCluskey Method of Minimization	Lecture		
<b>UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS</b>							
4	10-Jul-19	WED	4	Sequential logic	Lecture	ASS-II	T1
	11-Jul-19	THU	4,6	SR,JK Flip Flops,D,T flip flops	Lecture		T1
	12-Jul-19	FRI	8	Level triggering and Edge Triggering	Lecture		T1
5	15-Jul-19	MON	2	Counters	Lecture	ASS-II	T1
	17-Jul-19	WED	4	Asynchronous and Synchronous type	Lecture		T1
	18-Jul-19	THU	4	Modulo counters	Lecture		T1
	18-Jul-19	THU	6	Shift registers	Lecture		T2
	19-Jul-19	FRI	8	Design of synchronous sequential circuits	Lecture		T1
6	20-Jul-19	SAT	3	Moore and Melay models	Lecture	ASS-II	T1
	22-Jul-19	MON	2	Counters and State diagram	Lecture		T1
	1-Aug-19	THU	4	State reduction	Lecture		T1
1-Aug-19	THU	6	State assignment	Lecture	ASS-II	T1	
	1-Aug-19	THU	6				Static and Dyanamic RAM
<b>UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABILITY LOGIC DEVICES</b>							
6	2-Aug-19	FRI	8	Asynchronous sequential logic circuits	Lecture	ASS-II	T1
	3-Aug-19	SAT	3	Transition Stability	Lecture		T1
7	5-Aug-19	MON	2	Flow Stability	Lecture	ASS-II	T1
	7-Aug-19	WED	4	Race conditions	Lecture		T1
	8-Aug-19	THU	4	Hazards and errors in digital circuits	Lecture		T1
	8-Aug-19	THU	6	Analysis of asynchronous sequential logic circuit	Lecture		T1
	9-Aug-19	FRI	8	Introduction to programmable logic devices	Lecture		R1
8	12-Aug-19	MON	2	PROM	Lecture	ASS-II	T1
	14-Aug-19	WED	4	PLA	Lecture		T1
	15-Aug-19	THU	4	PAL	Lecture		T1
	15-Aug-19	THU	6	CPLD	Lecture		T1
16-Aug-19	FRI	8	FPGA	Lecture	T1		



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UNIT V VHDL										
9	26-Aug-19	MON	2	RTL design	Lecture	ASS-III	T1	12	12	
	28-Aug-19	WED	4	Combinational logic	Lecture		T1			
	29-Aug-19	THU	4	Sequential Circuit	Lecture		T1			
	29-Aug-19	THU	6	Operators	Lecture		T1			
	30-Aug-19	FRI	8	Introduction to packages	Lecture		T1			
	31-Aug-19	SAT	3	subprograms	Lecture					
10	5-Sep-19	THU	4	Test bench	Lecture		T2			
	5-Sep-19	THU	6	Test bench (Simulation/Tutorial Examples: adder)	Lecture		T3			
	6-Sep-19	FRI	8	Test bench (Simulation/Tutorial Examples: Counters)	Lecture		T3			
	7-Sep-19	SAT	3	Test bench (Simulation/Tutorial Examples: Flipflops)	Lecture		T3			
11	9-Sep-19	MON	4	Test bench (Simulation/Tutorial Examples: Mltiplexers)	Lecture		T3			
	10-Sep-19	TUE	1	Test bench (Simulation/Tutorial Examples: Demultiplexers)	Lecture		T3			

REFERENCES

BOOK NO	BOOK TITTLE	AUTHOR	PUBLISHER	EDITION
T1	Digital Electronics,	James W. Bignel	Cengage learning, 5th Edition	2007
T2	Digital Design with an introduction to theVHDL	M.Morris Mano	Pearson Education	2013
T3	Digital Logic & State Machine Design	Comer	McGraw Hill Edu	2012

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