PMC TECH

Er. PERUMAL MANIMEKALAI COLLEGE OF ENGINEERING
(Approved by AICTE & Affiliated to Anna University, Chennai)
(NAAC B++ Grade Institution, ISO 9001:2015 Certified Institution)
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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

Third Semester (Regulation 2013)

EE8351 DIGITAL LOGIC CIRCUITS

UNIT I

PART - A

1	What is variable mapping?	(2)	CO1 Remembering
2	What are prime implicates?	(2)	CO1 Remembering
3	Explain the De Morgan's theorem in Boolean Algebra.	(2)	CO1 Understanding
4	Determine (377)10 in octal and hexa-decimal equivalent.	(2)	CO1 Analyzing
5	What is K-map. List the limitations of K-map.	(2)	CO1 Remembering
6	List the factors used for measuring the performance of digital logic families.	(2)	CO1 Understanding
7	How does don't care condition in k-map help for circuit simplification.	(2)	CO1 Understanding
8	What do you mean by literal?	(2)	CO1 Remembering
9	Why are NAND and NOR gates known as universal gates?	(2)	CO1 Remembering
10	Define Tri-state gates.	(2)	CO1 Understanding
11	What is meant by weighted and non weighted code?	(2)	CO1 Remembering
12	List the applications of Gray code.	(2)	CO1 Remembering
13	Solve the subtraction using 1's complement: $(11010)_2$-$(10000)_2$	(2)	CO1 Applying
14	Classify the binary codes.	(2)	CO1 Understanding
15	Simplify (101101.1101) into decimal and Hexadecimal.	(2)	CO1 Analyzing
16	Classify the digital logic families.	(2)	CO1 Understanding
17	What is fan in and fan out?	(2)	CO1 Remembering
18	Define power dissipation.	(2)	CO1 Remembering
19	List the characteristics of ECL families.	(2)	CO1 Remembering
20	Outline the circuit diagram of NMOS NAND Gate with its truth table.	(2)	CO1 Understanding

PART B

1	Determine the single error correcting code for the information code 10111 for odd parity.	(13)	CO1 Evaluating
2	Explain in detail about error detection and correction codes.	(13)	CO1 Understanding
3	(a) Solve the following: (i) Binary into octal $(10101101.0111)_2$ (ii) Hexadecimal into binary $(36E.9A)_{16}$ (iii) Octal to hexadecimal $(615.28)_8$ (iv) Decimal into octal $(658.825)_{10}$ (v) 2's complement of $(11000100)_2$	(13)	CO1 Applying
4	Outline the schematic and explain the operation of RTL logic circuits.	(13)	CO1 Understanding
5	Explain the operation of DTL logic circuits with neat sketch.	(13)	CO1 Understanding
6	Explain the concept, operation and characteristics of CMOS technology.	(13)	CO1 Understanding
7	Given that the frame with bit sequence 1101011011 is transmitted. It has been received as 1101011010. Determine the Method of deducting the error using any one error deducting code.	(13)	CO1 Applying

PART C

1	(i) Deduct the odd parity hamming codes for the data 1 0 1 0. Introduce an error in the LSB of the hamming code and deduce the steps to deduct the error. (ii) The hamming code 1 0 1 1 0 1 1 0 1 is received. Correct it if any errors. There are four parity bits and odd parity is used.	(8) (7)	CO1 Applying
2	Compare the characteristics of TTL, ECL and CMOS logic families	(15)	CO1 Understanding
3	With circuit schematic and explain the operation and characteristics of ECL gate.	(15)	CO1 Understanding
4	With circuit schematic explain the operation of a two and three input TTL NAND gate with Totem pole	(15)	CO1 Understanding

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